REMARKS

Claims 1, 3-10, 12-18, 20-22, 24-26 and 28-29 remain in the present application. Claims 2, 11, 23 and 27 are cancelled herein. Claims 1, 3, 10, 14, 20, 24-25 and 28 are amended herein. Applicants respectfully submit that no new matter has been added as a result of the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

Claim Rejections – 35 U.S.C. §112

Claim 3 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter with Applicant regards as the invention. More specifically, the rejection states that there is insufficient antecedent basis for "said device" in Claim 3.

Claim 3 is amended herein. Applicant respectfully submits that Claims 3 complies with the requirements of 35 U.S.C. §112, second paragraph, in light of the claim amendments.

Claim Rejections – 35 U.S.C. §102

Claims 1-3, 6-11, 15-18, 20 and 23-29 are rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent Number 6,347,344 to Baker et al. (hereafter referred to as "Baker"). Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 1-3, 6-11, 15-18, 20 and 23-29 are neither anticipated nor rendered obvious by Baker for the following reasons.

Applicants respectfully direct the Examiner to independent Claim 1 that recites a data and communication apparatus communicatively coupled with a multi-processor shared memory multimedia chip system for providing interprocessor communication while enhancing performance of each processor integral with the multi-processor shared memory multimedia chip system, the data and communication apparatus comprising (emphasis added):

> a data memory to retrievably store data;
> an instruction memory coupled with said data memory to retrievably store instructions;
> an incoming buffer coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus, said incoming buffer further adapted to provide fast access to streaming data and perform prefetch operations;
> an outgoing buffer coupled with said data memory and said instruction memory which monitors and permits transfer of data out of said data and communication apparatus, said outgoing buffer enables said each processor to communicate with other processors disposed within said system; and
> multiple registers coupled with said data and communication apparatus, said registers adapted to provide enhanced configurability and control of said data memory and said instruction memory, said registers further adapted to provide addressable memory storage locations for said retrievably stored data and said retrievable stored instructions, said registers separate from and in addition to the registers within said multi-processor shared memory multimedia chip system.

Claims 2, 11, 23 and 27 are cancelled herein, and therefore, Applicants respectfully submit that the 35 U.S.C. §103(a) rejections corresponding to Claims 2, 11, 23 and 27 are moot. Independent Claims 10 and 20 recite similar limitations to independent Claim 1. Claims 3-9 and 29 depend from independent Claim 1 and recite further limitations to the claimed invention. Claims 12-18 depend from independent Claim 10 and recite further limitations to the claimed invention. Claims 21-22, 24-26 and 28 depend from independent Claim 20 and recite further limitations to the claimed invention.

Applicants respectfully submit that Baker fails to teach or suggest the limitation of "said incoming buffer further adapted to... perform prefetch operations" as recited in independent Claim 1. As recited in the present application, a data and communication apparatus comprises an incoming buffer adapted to perform prefetch operations.

In contrast to the claimed embodiments, Applicants understand the cited portion of Baker to teach data buffer 206 without the ability to perform prefetch operations (Figure 11; col. 37, lines 20-27). Although buffer 206 may buffer data input to DMA controller 138 as shown in Figure 11, Applicants respectfully submit that Baker is silent as to buffer 206 performing prefetch operations as claimed.

Moreover, Baker teaches away from the claimed embodiments by teaching that data streamer 122, as opposed to buffer 206, performs prefetch operations (col. 29, lines 26-31). Additionally, Applicants would also like to point out that data streamer 122 also fails to teach or suggest an incoming buffer as claimed given that Baker expressly teaches that data streamer 122 "is employed for predetermined data movements *within* multimedia processor 100" (col. 19, lines 3-5). As such, Baker further teaches away from the claimed embodiments by teaching that data streamer 122 transfers data within multimedia processor 100 instead of permitting the transfer of data into the data and communication apparatus as claimed.

Applicants respectfully submit that Baker fails to teach or suggest the limitation of "said outgoing buffer enables said each processor to communicate with other processors disposed within said system" as recited in independent

Claim 1. As recited in the present application, a data and communication apparatus comprises an outgoing buffer enabling each processor of the data and communication apparatus to communicate with other processors within the system.

In contrast to the claimed embodiments, Applicants understand Baker to teach data buffer 208 for buffering data sent to I/O devices (col. 37, lines 35-38). However, Applicants respectfully submit that Baker does not teach or suggest that buffer 208 enables interprocessor communication as claimed. Furthermore, Applicants also submit that the cited sections of Baker teaching simultaneous data transfers (col. 4, lines 8-16) also do not teach or suggest interprocessor communication as claimed. For example, Baker expressly teaches that the simultaneous data transfers occur *within* the multimedia processor instead of between processors as claimed (col. 4, line 10).

Applicants respectfully submit that Baker fails to teach or suggest the limitation of "said registers adapted to provide enhanced configurability and control of said data memory and said instruction memory" as recited in independent Claim 1. As recited in the present application, a plurality of registers are adapted to provide enhanced configurability and control of data memory and instruction memory.

In contrast to the claimed embodiments, Applicants understand the cited portion of Baker to teach I/O units with a corresponding control register to enable control of the I/O units (col. 12, lines 27-32). As such, Baker expressly teaches away from the claimed embodiments by teaching registers to enable control of I/O units instead of data memory and instruction memory as claimed.

For these reasons, Applicants respectfully submit that independent Claim 1 is neither anticipated nor rendered obvious by Baker, thereby overcoming the 35 U.S.C. §102(e) rejection of record. Since independent Claims 10 and 20 contain limitations similar to those discussed above with respect to independent Claim 1, independent Claims 10 and 20 also overcome the 35 U.S.C. §102(e) rejections of record. Since dependent Claims 3-9, 12-18, 21-22, 24-26 and 28-29 recite further limitations to the invention claimed in their respective independent Claims, Claims 3-9, 12-18, 21-22, 24-26 and 28-29 are also neither anticipated nor rendered obvious by Baker. Thus, Claims 1, 3, 6-10, 15-18, 20, 24-26 and 28-29 are therefore allowable.

Claim Rejections – 35 U.S.C. §103

Claims 4, 13 and 21

Claims 4, 13 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Baker in view of United States Patent Number 5,892,966 to Petrick et al. (hereafter referred to as "Petrick"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 4, 13 and 21 are not rendered obvious by Baker in view of Petrick for the following reasons.

The rejection states that Baker fails to teach or suggest the limitations of "wherein said data said retrievably stored in said data memory is an interrupt service routine, wherein access to retrieve said interrupt service routine is via said I/O space, such that traffic on said memory space is commensurately

reduced, so as to ensure the time required to complete said interrupt service routine" as recited in Claim 4. Applicants concur.

Applicants respectfully submit that that Petrick, either alone or in combination with Baker, fails to cure the deficiencies of Baker discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Petrick also fails to teach or suggest the limitations of "said incoming buffer further adapted to... perform prefetch operations," "said outgoing buffer enables said each processor to communicate with other processors disposed within said system," and "said registers adapted to provide enhanced configurability and control of said data memory and said instruction memory" as recited in independent Claim 1.

Furthermore, Applicants respectfully submit that Petrick fails to teach or suggest the limitations of "wherein access to retrieve said interrupt service routine is via said I/O space, such that traffic on said memory space is commensurately reduced, so as to ensure the time required to complete said interrupt service routine" as recited in Claim 4. Applicants understand Petrick to teach a visible register set coupled between a hardware and a multimedia processor, where the visible register set "allows the two distinct processors to work together with a reduced amount of interface circuitry" and enable each processor to control the other (col. 8, lines 47-57). As such, assuming arguendo that the visible register set taught by Petrick enables access to interrupt service routines via I/O space as claimed, Applicants respectfully submit that such access is to reduce interface circuitry and allow processors control over other processors instead of reducing traffic on memory space and reducing the time to complete an interrupt service routine as claimed.

For these reasons, Applicants respectfully submit that Claim 4 is not rendered obvious by Baker in view of Petrick, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since Claims 13 and 21 recite similar limitations to those in Claim 4, Claims 13 and 21 also overcome the 35 U.S.C. §103(a) rejections of record. Thus, Claims 4, 13 and 21 are therefore allowable.

Claims 5, 14 and 22

Claims 5, 14 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Baker in view of United States Patent Number 4,386,402 to Toy (hereafter referred to as "Toy"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 5, 14 and 22 are not rendered obvious by Baker in view of Toy for the following reasons.

The rejection states that Baker fails to teach or suggest the limitations of "wherein said data retrievably stored in said data memory unit is real-time kernel thread context data, wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space in commensurately reduced, so as to increase speed with which thread context switching is achieved" as recited in Claim 5. Applicants concur.

Applicants respectfully submit that that Toy, either alone or in combination with Baker, fails to cure the deficiencies of Baker discussed above with respect to independent Claim 1. Specifically, Applicants respectfully submit that Toy also fails to teach or suggest the limitations of "said incoming buffer further adapted

to... perform prefetch operations," "said outgoing buffer enables said each processor to communicate with other processors disposed within said system," and "said registers adapted to provide enhanced configurability and control of said data memory and said instruction memory" as recited in independent Claim 1.

For these reasons, Applicants respectfully submit that Claim 5 is not rendered obvious by Baker in view of Toy, thereby overcoming the 35 U.S.C. §103(a) rejection of record. Since Claims 14 and 22 recite similar limitations to those in Claim 5, Claims 14 and 22 also overcome the 35 U.S.C. §103(a) rejections of record. Thus, Claims 5, 14 and 22 are therefore allowable.

CONCLUSION

Applicants respectfully submit that Claims 1, 3-10, 12-18, 20-22, 24-26 and 28-29 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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